

REMARKS

Applicants submit that entry of this Amendment is proper under 37 CFR §1.116, since no new claims or issues are presented. That is, the amendments to claims 3 and 6 attempt to find wording acceptable to the Examiner.

However, it is noted that Applicants believe that the Examiner's broad interpretation of the previous claim language is not reasonable because it ignores the plain meaning of the claim language, as further explained below. Indeed, Applicants are willing to proceed to Appeal with the previous wording. Applicants further submit that the Examiner's initial burden has not been met even with the previous claim wording but are attempting to expedite prosecution. Entry of this Amendment reduces issues for Appeal, since claims 3 and 6 are now clearly allowable over the prior art of record, even in view of the Examiner's overly-broad interpretation of claim language.

It is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 2-25 are all of the claims pending in the present Application. Claims 7-21 are allowed. Claims 2-6 and 23 stand rejected under 35 USC §102(e) as unpatentable anticipated by US Patent 6,499,048 to Williams, and claims 24 and 25 stand rejected under 35 USC §103(a) as unpatentable over Williams.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described, for example, by independent claim 4 and similarly in claims 23-25, the present invention is directed to a method of multithread processing on a computer. A first thread is processed on a first component. The first component is capable of simultaneously executing at least two threads. The first thread is also processed on a second component, and the second component is also capable of simultaneously executing at least two threads.

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A result of the processing on the first component is compared with a result of the processing on the second component. The processing of the thread on the second component is performed at a priority lower than a priority of the processing of the thread on the first component.

Since lower priority generally results in slower execution, this scheme of prioritization of the present invention has the advantage of intentionally keeping one thread on one component behind its sister thread on the other component. By intentionally making one thread lag behind, the efficiency of the combined computing resources of the two components can be enhanced, since the lagging thread processing can take advantage of the processing experience of the same thread as executed by the other component.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Williams anticipates claims 2-6 and 23 and renders obvious claims 24 and 25. Applicants respectfully disagree.

It appears that the Examiner continues not to appreciate the distinct differences between the claimed invention and Williams.

In the case of claim 3, Williams does a disabling from the point of view of "graceful degradation" (e.g., to allow the processor to continue functioning without fault tolerance when a redundant unit has failed).

In contrast, the aspect of the present invention described by claim 3 describes a capability that such disabling allows different programs to be run on the processors when high throughput is needed. Thus, in the present invention, the disabling is a control given to the user of the system, rather than one which results from a failure in the system.

Moreover, in the present invention, it is not the processor that is disabled by the disabling signal. Rather, as clearly described even before the wording change of the present invention, it is the feature of using the processors in a redundant manner that disabled. This distinction was pointed out in the previous Amendment and Applicants are comfortable proceeding to Appeal with this previous wording.

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Relative to claims 4 and 5, the comments made in the previous Amendment still stand and are not repeated herein for sake of brevity, except as augmented, as follows.

To begin with, the difference between the present invention and Williams is analogous to the difference between two cars that are traveling close to each other on a one-lane road, with the second behind the first, versus the scenario in which the same two cars are running close to each other on a two lane road, where there is no guarantee that the second will not at some point get ahead of the first.

That is, Applicants submit that the term "higher priority" is a term of art that cannot be discounted by the Examiner. In Williams, there is no concept of priority in which it is assured that one processor will proceed through the thread processing at a defined higher priority.

An advantage of clearly defining a priority for the two processings is that the higher-priority processing can provide guidance to the lower-priority processing for decision points that will eventually be encountered by the lower-priority processing and whose outcomes are already known to the higher-priority processing. Williams fails to suggest this feature.

Relative to claim 6, although it is arguable that Williams can be described as "using information about the processing" of each of the two processes, Applicants submit that one of ordinary skill in the art could not agree with the Examiner that it is reasonable to describe that Williams' technique describes that "one of the processors uses information available from the processing of the thread on another processor", as is required by the plain meaning of the claim language. Applicants have attempted to reword the claim language to be more acceptable to the Examiner, in a good faith effort to expedite prosecution, but point out that they are also satisfied to proceed to Appeal with the previous wording, pointing out that the evaluation of record fails to heed the plain meaning of the claim language and the prior art description.

That is, in Williams, the "progress indication" described at lines 22-25 of column 5 is consumed by the monitor, not by the other processor, as required by the previous claim

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language. In Williams, the "progress indication" information is used only (by the monitor, not one of the processors) to control the speed of execution of the second component. In fact, for the same program, in Williams, it may sometimes be the case that the same information is used to control the speed of the FIRST component. Hence, Applicants submit that the Examiner fails to meet the initial burden of meeting the "all limitations" requirement of a *prima facie* rejection.

In contrast to Williams, in the present invention, it is only the low priority thread processing that is ever controlled using information provided by the high priority thread processing. Moreover, the information that is used by the low-priority thread is used in the present invention for actually controlling the internal functional paths of the second thread, not for controlling its speed of processing. In the present invention, the high priority thread does not need information from the low priority thread for its execution.

Returning again to the earlier analogy, the present invention provides a method similar to that of the first car in the one-lane example being able to provide functional information, for example, whether the headlights or the directional indicators should be turned on, to the car following it. The concept of higher priority of the present invention is analogous to the speed of the second car being automatically limited simply because it is behind the first car and there is no passing lane.

Relative to the rejection for claim 5, the most that can be asserted about Williams is that one processor or the other will likely be lagging, but it cannot reasonably be alleged that a first processor positively will be lagging a second processor, as required by the plain meaning of the claim language. That is, it is just as likely in Williams that the second processor will lag the first processor.

Hence, turning to the clear language of the claims, in Williams there is no teaching or suggestion of: "... wherein an input selectively enables or disables said comparing", as required by claim 3.

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Relative to claims 4 and 23-25, in Williams there is no teaching or suggestion of: "... wherein said processing said thread on said second component is performed at a priority lower than a priority of said processing said thread on said first component."

Relative to claim 5, in Williams there is no teaching or suggestion of: "... wherein said processing said thread on said second component occurs at a time delayed from that of said processing said thread on said first component."

Relative to claim 6, in Williams there no teaching or suggestion of: "... uses information about an outcome of executing an instruction that is available from said processing said thread on said first component at said higher priority."

For the reasons stated above, Applicants respectfully submit that the claimed invention is fully patentable over the cited reference Williams.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicants submit that claims 2-25, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

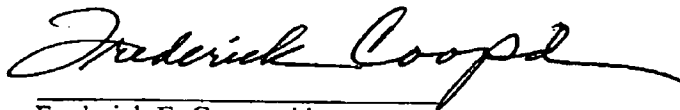
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The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 3/28/05

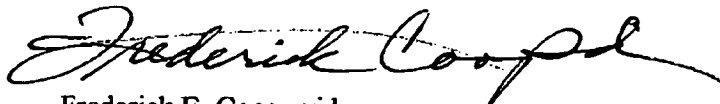


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CERTIFICATION OF TRANSMISSION

I certify that I transmitted via facsimile to (703) 872-9306 this Amendment under 37 CFR §1.116 to Examiner G. Chu on March 28, 2005.



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